

CLAIMS

What is claimed is:

1 1. A delay circuit, comprising:
2 a first circuit having a circuit input to receive a reference signal and a circuit
3 output to output a delayed signal;
4 a falling edge delay circuit coupled to the first circuit to control delay of a falling
5 edge of the reference signal; and
6 a rising edge delay circuit coupled to the first circuit to control delay of a rising
7 edge of the reference signal.

1 2. The delay circuit of claim 1, wherein the first circuit comprises an enable
2 circuit further including an enable input to enable the delay circuit.

1 3. The delay circuit of claim 2, wherein the circuit input comprises a clock input
2 to receive a reference clock signal and the reference signal comprises the reference clock
3 signal.

1 4. The delay circuit of claim 3, wherein the falling edge delay circuit and the
2 rising edge delay circuit are coupled to delay the falling edge and the rising edge
3 independently of each other.

1 5. The delay circuit of claim 4, wherein the falling edge delay circuit is further
2 coupled to selectively delay the falling edge of the reference clock signal by variable
3 falling delays and wherein the rising edge delay circuit is further coupled to selectively
4 delay the rising edge of the reference clock signal by variable rising delays.

1 6. The delay circuit of claim 5, wherein the falling edge delay circuit further
2 comprises falling delay inputs to receive falling delay signals, the falling edge delay
3 circuit to select one of the variable falling delays based on the falling delay signals and
4 wherein the rising edge delay circuit further comprises rising delay inputs to receive
5 rising delay signals, the rising edge delay circuit to select one of the variable rising delays
6 based on the rising delay signals.

1 7. The delay circuit of claim 5, wherein the falling edge delay circuit is further
2 coupled to selectively delay the falling edge of the reference clock signal by one of four
3 falling delays in linear increments, and wherein the rising edge delay circuit is further
4 coupled to selectively delay the rising edge of the reference clock signal by one of four
5 rising delays in linear increments.

1 8. The delay circuit of claim 6, wherein the enable circuit comprises:
2 a NAND logic gate having first and second NAND inputs and a NAND output,
3 the first NAND input coupled to the clock input and the second NAND input coupled to
4 the enable input;

5 a first pull up path including a first transistor to selectively couple the NAND
6 output to the falling edge delay circuit;
7 a pull down path including second and third transistors coupled in series to
8 selectively couple the NAND output to the rising edge delay circuit; and
9 an inverter coupling the NAND output to the circuit output.

1 9. The delay circuit of claim 8, wherein the falling edge delay circuit comprises
2 three parallel pull up paths each including at least one transistor to be coupled between a
3 supply voltage and the first pull up path of the enable circuit, each one of the three
4 parallel pull up paths responsive to the falling delay signals to select one of the variable
5 falling delays.

1 10. The delay circuit of claim 8, wherein the rising edge delay circuit comprises
2 three parallel pull down paths each including at least one transistor to be coupled between
3 a ground voltage and the first pull down path of the enable circuit, each one of the three
4 parallel pull down paths responsive to the rising delay signals to select one of the variable
5 rising delays.

1 11. The delay circuit of claim 4, wherein the enable circuit is an inverting enable
2 circuit to invert the reference clock signal, the inverting enable circuit comprising:
3 a NAND logic gate having first and second NAND inputs and a NAND output,
4 the second NAND input coupled to the enable input;
5 a first inverter coupling the clock input to the first NAND input;

6 a pull up path including a first transistor to selectively couple the NAND output to
7 the rising edge delay circuit;

8 a pull down path including second and third transistors coupled in series to
9 selectively couple the NAND output to the falling edge delay circuit; and

10 an second inverter coupling the NAND output to the circuit output.

1 12. The delay circuit of claim 11, wherein the rising edge delay circuit comprises
2 three parallel pull up paths each including at least one transistor to be coupled between a
3 supply voltage and the first pull up path of the enable circuit, each one of the three
4 parallel pull up paths responsive to rising delay inputs of the rising edge delay circuit to
5 select one of variable falling delays of the output delayed signal.

1 13. The delay circuit of claim 11, wherein the falling edge delay circuit
2 comprises three parallel pull down paths each including at least one transistor to be
3 coupled between a ground voltage and the first pull down path of the enable circuit, each
4 one of the three parallel pull down paths responsive to falling delay inputs of the falling
5 edge delay circuit to select one of variable rising delays of the output delayed signal.

1 14. A machine-accessible medium having contained thereon a description of an
2 integrated circuit, the integrated circuit comprising:

3 a clock enable circuit having a clock input to receive a reference clock signal, an
4 enable input, and a circuit output to output a delayed clock signal;

5 a falling edge delay circuit coupled to the enable circuit to control delay of a
6 falling edge of the reference clock signal; and
7 a rising edge delay circuit coupled to the enable circuit to control delay of a rising
8 edge of the reference clock signal.

1 15. The machine-accessible medium of claim 14, wherein the falling edge delay
2 circuit and the rising edge delay circuit are coupled to delay the falling edge and the
3 rising edge independently of each other.

1 16. The machine-accessible medium of claim 15, wherein the falling edge delay
2 circuit is further coupled to selectively delay the falling edge of the reference clock signal
3 by variable falling delays and wherein the rising edge delay circuit is further coupled to
4 selectively delay the rising edge of the reference clock signal by variable rising delays.

1 17. The machine-accessible medium of claim 16, wherein the falling edge delay
2 circuit further comprises falling delay inputs to receive falling delay signals, the falling
3 edge delay circuit to select one of the variable falling delays based on the falling delay
4 signals and wherein the rising edge delay circuit further comprises rising delay inputs to
5 receive rising delay signals, the rising edge delay circuit to select one of the variable
6 rising delays based on the rising delay signals.

1 18. The machine-accessible medium of claim 16, wherein the falling edge delay
2 circuit is further coupled to selectively delay the falling edge of the reference clock signal

3 by one of four falling delays in linear increments, and wherein the rising edge delay
4 circuit is further coupled to selectively delay the rising edge of the reference clock signal
5 by one of four rising delays in linear increments.

1 19. The machine-accessible medium of claim 17, wherein the clock enable circuit
2 comprises:

3 a NAND logic gate having first and second NAND inputs and a NAND output,
4 the first NAND input coupled to the clock input and the second NAND input coupled to
5 the enable input;

6 a first pull up path including a first transistor to selectively couple the NAND
7 output to the falling edge delay circuit;

8 a pull down path including second and third transistors coupled in series to
9 selectively couple the NAND output to the rising edge delay circuit; and

10 an inverter coupling the NAND output to the circuit output.

1 20. The machine-accessible medium of claim 19, wherein the falling edge delay
2 circuit comprises three parallel pull up paths each responsive to the falling delay signals
3 to select one of the variable falling delays, and wherein the rising edge delay circuit
4 comprises three parallel pull down paths each responsive to the rising delay signals to
5 select one of the variable rising delays.

1 21. The machine-accessible medium of claim 14, wherein the description
2 comprises one of hardware behavioral code, register transfer level code, a netlist, and a
3 circuit layout.

1 22. An integrated circuit, comprising:
2 a clock distribution network to distribute a reference clock signal throughout the
3 integrated circuit;
4 clock delay circuits each comprising:
5 a clock enable circuit having a clock input to receive the reference clock
6 signal and a circuit output to output a delayed clock signal;
7 a falling edge delay circuit coupled to the enable circuit to control delay
8 of a falling edge of the reference clock signal; and
9 a rising edge delay circuit coupled to the enable circuit to control delay
10 of a rising edge of the reference clock signal;
11 latches each clocked according to the delayed clock signal output from each of the
12 clock delay circuits; and
13 logic clusters to compute logic values, the latches coupled to buffer the logic
14 values between clock edges of the delayed clock signals.

1 23. The integrated circuit of claim 22, wherein the falling edge delay circuit and
2 the rising edge delay circuit are coupled to delay the falling edge and the rising edge
3 independently of each other.

1 24. The integrated circuit of claim 22, wherein the falling edge delay circuit
2 further comprises falling delay inputs to receive falling delay signals, the falling edge
3 delay circuit to selectively delay the falling edge of the reference clock signal by one of
4 variable falling delays based on the falling delay signals, and wherein the rising edge
5 delay circuit further comprises rising delay inputs to receive rising delay signals, the
6 rising edge delay circuit to selectively delay the rising edge of the reference clock signal
7 by one of the variable rising delays based on the rising delay signals.

1 25. The integrated circuit of claim 24, wherein the clock delay circuits are
2 grouped into domains of the integrated circuit, the falling delay inputs and the rising
3 delay inputs of the clock delay circuits coupled to receive the same falling delay signals
4 and the same rising delay signals within each of the domains.

1 26. The integrated circuit of claim 24, wherein the falling edge delay circuit is
2 further coupled to selectively delay the falling edge of the reference clock signal by one
3 of four falling delays in first increments, and wherein the rising edge delay circuit is
4 further coupled to selectively delay the rising edge of the reference clock signal by one of
5 four rising delays in second increments.

1 27. The integrated circuit of claim 26, wherein the first and second increments
2 comprise substantially linear increments.

1 28. The integrated circuit of claim 22, wherein the integrated circuit comprises a
2 microprocessor.

1 29. The integrated circuit of claim 22, wherein the logic clusters comprise at least
2 one of combinational logic and sequential logic.

1 30. The integrated circuit of claim 23, wherein the clock enable circuit
2 comprises:

3 a NAND logic gate having first and second NAND inputs and a NAND output,
4 the first NAND input coupled to the clock input and the second NAND input coupled to
5 the enable input;

6 a first pull up path including a first transistor to selectively couple the NAND
7 output to the falling edge delay circuit;

8 a pull down path including second and third transistors coupled in series to
9 selectively couple the NAND output to the rising edge delay circuit; and

10 an inverter coupling the NAND output to the circuit output.

1 31. The integrated circuit of claim 30, wherein the falling edge delay circuit
2 comprises three parallel pull up paths each responsive to the falling delay signals to select
3 one of the variable falling delays, and wherein the rising edge delay circuit comprises
4 three parallel pull down paths each responsive to the rising delay signals to select one of
5 the variable rising delays.

- 1 32. The integrated circuit of claim 22, wherein the latches comprise flip-flops.